IN THE CLAIMS

Cancel Claims 15, 16, 19 and 20 without prejudice, amend Claims 1, 5 and 12-14 as follows and add Claims 21-24:

1. (Currently Amended) Method of operating multiple (n) parallel-connected pulse-controlled inverters (1,2), ~~characterized in that~~ wherein

the individual current(s) of the (n) pulse-controlled inverters (1,2) , or of a number reduced by 1 (n-1) of pulse-controlled inverters (1,2) is/are regulated, and each pulse-controlled inverter (1, 2) includes first (IGBT T11, IGBT T21) and second (IGBT T14, IGBT T24) insulated gate bipolar transistors and first (D11, D21) and second (D14, D24) diodes each connected in parallel with a respective one of the first (IGBT T11, IGBT T 21) and second (IGBT T14, IGBT T24) insulated gate bipolar transistors in the direction of reverse voltage (UD-) to forward voltage (UD+).

2. (Original) Method according to Claim 1, characterized in that the individual currents from two pulse-controlled inverters (1, 2) are regulated.

3. (Previously presented) Method according to Claim 1, characterized by pulse-controlled inverters (1, 2) of the same output.

4. (Original) Method according to Claim 3, characterized in that the total current is uniformly distributed among pulse-controlled inverters (1, 2) of the same output.

5. (Currently Amended) Method according to Claim 1, ~~characterized in that~~ wherein each pulse-controlled inverter is regulated separately, with each regulator having sensed currents to separately adjust each regulator.

6. (Previously presented) Method according to Claim 1, characterized in that the input variable of regulation is generated by the difference between the setpoint value and the actual value of the corresponding output current, and by the modulation pattern.

7. (Previously presented) Method according to Claim 1, characterized in that the control edges of the power semiconductors (T11, T14, T21, T24) are shifted within the pulse-controlled inverter(s) (1, 2).

8. (Previously presented) Method according to Claim 1, characterized in that each phase of one, of multiple, or of all pulse-controlled inverters (1, 2) is regulated individually.

9. (Previously presented) Method according to Claim 1, characterized in that the gain factors (K1, K2) of regulation are dependent on external limiting conditions.

10. (Previously presented) Method according to Claims 2 characterized by pulse-controlled inverters (1, 2) of the same output.

11. (Previously presented) Method according to Claim 10, characterized in that the total current is uniformly distributed among pulse-controlled inverters (1, 2) of the same output.

12. (Currently amended) Method according to Claim 2, characterized in that each pulse-controlled inverter (1, 2) is regulated separately, with each regulator having sensed currents to separately adjust each regulator.

13. (Currently amended) Method according to Claim 3, characterized in that each pulse-controlled inverter (1, 2) is regulated separately, with each regulator having sensed currents to separately adjust each regulator.

14. (Currently amended) Method according to Claim 4, characterized in that each pulse-controlled inverter (1, 2) is regulated separately, with each regulator having sensed currents to separately adjust each regulator.

Claims 15 and 16. Canceled.

17. (Previously presented) Method according to Claim 2, characterized in that the input variable of regulation is generated by the difference between the setpoint value and the actual value of the corresponding output current, and by the modulation pattern.

18. (Previously presented) Method according to Claim 3, characterized in that the input variable of regulation is generated by the difference between the setpoint value and the actual value of the corresponding output current, and by the modulation pattern.

Claims 19 and 20. Canceled.

21. (New) Method according to Claim 6, wherein for each pulse-controlled inverter (1, 2),

when the actual value of current (I11, I21) is greater than the setpoint value, a turn-on edge of the first transistor (T11, T21) and turn-off edge of the second transistor (T14, T24) are each delayed, a turn-off edge of the first transistor (T11, T21) and turn-on edge the second transistor (T14, T24) remaining undelayed,

when the actual value of the current (I11, I21) is smaller than the setpoint value, the turn-on edge of the first transistor (T11, T21) and turn-off edge of the second transistor (T14, T24) are undelayed, with the turn-off edge of the first transistor (T11, T21) and turn-on edge of the second transistor (T14, T24) each being delayed, and

when the actual value of the current (I11, I21) equals the setpoint value, the turn-on edges and turn-off edges of the first (T11, T21) and second (T14, T24) transistors all remain undelayed.

22. (New) Method according to Claim 21, wherein upon asymmetrical distribution of current, said two pulse-controlled inverters (1,2) have setpoint/actual-value deviations of opposite polarity.

23. (New) Method according to Claim 21, wherein when the actual value of the current (I11) in one (1) of the inverters (1, 2) is excessively larger than the actual value of the current (I21) in the other (2) of the inverters (1,2), different switching time points produce a voltage-time integral at respective output chokes (3, 6), resulting in a current change in the two chokes (3,6) in a direction of removing setpoint/actual value deviation, such that total current remains unchanged.

24. (New) Method according to Claim 21, wherein

the actual values of current (I11, I21) are summed in a summing element (8),

the resulting sum is sent to respective amplifiers (9, 10), where the sum is amplified by respective gain factors (K1, K2),

output of each said amplifier (9, 10) is forwarded to a respective differentiating element (11, 13) in which difference (12, 14) between the amplifier output and actual current (I11, I21) is taken,

both said differences (12, 14) are then fed to a regulator (15) to which a modulation pattern (16) is also supplied, and

the regulator (15) generates control pulses for the transistors (T11, T14, T21, T24).